## REMARKS

### Amendment to the claims

The language of claims 2-6, 7-13 and 15-20 has been clarified to recite "the method of ~~as claimed in~~".

Claim 21 has been cancelled without prejudice.

The language of claims 23 and 24 has been amended to recite that the silicon etching agent comprises "*$Cl_2$, $SF_6$, or HBr*". These amendments are supported by the application as filed, for example the third paragraph of page 4 and the paragraph bridging pages 4 and 5.

No new matter was added.

### Rejection under 35 U.S.C. 112

Claims 21, 23, and 24 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The Applicants have cancelled claim 21 and amended claims 23 and 24 to recite that "*said silicon etching agent comprises $Cl_2$, $SF_6$, or HBr*". The Applicants note that, as detailed above, the new language of claims 23, 24 is supported by the application as filed, and respectfully request the Examiner to withdraw the present rejection.

Rejection under 35 U.S.C. 103

Claims 1-3, 5-10, 12-15 and 17-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,204,130 to Gardner in view of U.S. Patent No. 5,395,804 to Ueda and admitted prior art. Claims 4, 11 and 16 stand rejected rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner, Ueda and admitted prior art, and further in view of U.S. Patent No. 5,977,589 to Schloesser. The Applicants respectfully disagree.

**Claim 1**

In the present action, the Examiner acknowledges that Gardner does not describe using a silicon etching agent as recited in claim 1.

However, the Examiner notes that Ueda (U.S. 5,395,804) teaches oxidizing a polysilicon layer using oxygen and HCl, and asserts that it would have been obvious "to modify Gardner's oxidizing mixture by adding HCl because Ueda teaches that chlorine would diffuse in the polysilicon film and dangling bonds would be terminated by halogen atoms (col. 4, line 15--18)".

The applicants disagree with the Examiner and note that Ueda relates to manufacturing a TFT having a polysilicon channel region with excellent cristalinity to reduce the leakage current that is *"thought to originate from field emission of carriers through trap states in the grain boundaries of drain junction regions in the TFT"* (column 1, lines 23-25).

As noted by the Examiner, such improved cristalinity is obtained by terminating the dangling bonds in the polysilicon of the channel region with halogen atoms. However, Ueda unambiguously teaches that improving the cristalinity of the channel region aims at reducing leakage current in drain junction regions of the channel region.

On another hand, Gardner teaches (see abstract) forming a semiconductor device having a reduced polysilicon gate electrode width. Gardner obtains this reduced gate width by:

-forming a polysilicon block over an insulating film;

-oxidizing the polysilicon block to grow an oxide layer on exposed surfaces of the polysilicon block and thereby reduce the width of the polysilicon block; and

-removing the oxide layer to form a gate electrode with the remaining portion of the polysilicon block.

The Applicants note that the "oxidizing mixture" of Gardner is used in the above steps for forming the gate electrode. The Applicants note that the gate electrode of Gardner is isolated from a channel region (by an insulating layer 205, see Figure 2G), and note that the Examiner has failed to show how, why or where leakage current such as in Ueda's channel would develop in the gate electrode of Gardner.

Since there is no apparent leakage current in the gate electrode of Gardner, there is no motivation to modify the gate electrode of Gardner to reduce such leakage currents. Since Ueda relates to reducing leakage currents, there is in particular no motivation to modify the steps for forming the gate electrode of Gardner with the teachings of Ueda.

At least for the above reason, the Applicants respectfully submit that contrary to the Examiner's assertion, one skilled in the art would have lacked motivation to modify the "oxidizing mixture" used for manufacturing the gate electrode of Gardner in view of the teachings of Ueda.

Further, the Applicants note that the Ueda reference discloses treating the surface of a polysilicon layer by terminating the dangling bonds in the surface of the polysilicon layer in the channel region of a TFT device.

On the other hand, Gardner discloses oxidizing the surface of a polysilicon block forming a gate electrode and then removing the oxidized surface to obtain a gate electrode having a reduced width. Gardner further teaches submitting the surface of the

etched polysilicon block (209A, see Fig. 2F) to etching materials in at least two subsequent steps: the etching of layers 207 & 205 under block 209A such as in Fig. 2G; and the etching of spacers 219 on the sides of block 209A such as in Fig. 2I. The Applicants submit that such subsequent steps are also bound to remove part of the exposed surface of the etched polysilicon block 209A.

The Applicants respectfully submit that it would make no sense to use Ueda's "oxidizing mixture" when oxidizing the surface of Gardner's polysilicon to remove the dangling bonds thereof, because if subsequent removals of the surface of the polysilicon occur, such as taught by Gardner, the removal of the surface of the polysilicon gate would involve removal of the portions of the polysilicon gate where the dangling bonds have been terminated, and would yield a polysilicon gate electrode still having dangling bonds.

For this reason also, the Applicants respectfully submit that the skilled person would have lacked motivation for combining Ueda and Gardner.

In addition, the Applicants note that Ueda was granted in March 1995, more than two years before the filing, in August 29, 1997, of Gardner. The Applicants respectfully submit that, if it were obvious to combine Gardner and Ueda, as opined by the Examiner, the inventors of Gardner would have done so.

At least in view of the above, the Applicants respectfully submit that claim 1 is patentable over Gardner and Ueda.

**Claims 7 and 14**

Applicants respectfully submit that the above arguments can be used to show that Gardner and Ueda, as well as the admitted prior art, fail to disclose or suggest:

a method as recited in claim 7, and in particular comprising "*treating the patterned silicon layer with patterns and etching residues on sidewalls thereof using a gas comprising oxygen and a silicon etching agent, forming an etching*

*buffer layer conformally on the etching residues and the top layer of the patterned silicon layer*"; or

a method as recited in claim 14, and in particular comprising "*introducing a gas containing oxygen treatment, using a gas comprising oxygen and a silicon etching agent, to conformally form an etching buffer layer on the surface etching residues and the top layer of the patterned silicon layer*".

Accordingly, Applicants respectfully submit that claims 7 and 14 are patentable over Gardner in view of Ueda and further in view of the admitted prior art.

**Claims 2-3, 5-6, 8-10, 12-13, 15, 17-20, 22-24**

Claims 2-3, 5-6 and 22 depend directly or indirectly on claim 1; claims 8-10, 12-13 and 23 depend directly or indirectly on claim 7, and claims 15, 17-20 and 24 depend directly on claim 14. Applicants respectfully submit that at least in view of their dependency on claims 1, 7 or 14, claims 2-3, 5-6, 8-10, 12-13, 15, 17-20 and 22-24 are patentable over Gardner in view of Ueda and further in view of the admitted prior art.

**Claims 4, 11 and 16**

Claim 4 depends on claim 1, claim 11 depends on claim 7, and claim 16 depends on claim 14. Applicants respectfully submit that the Examiner has failed to show that Schloesser discloses or suggests:

a method as recited in claim 1, and in particular comprising "*treating said patterned silicon layer with etching residues on sidewalls thereof using a gas comprising oxygen and a silicon etching agent to thereby form an etching buffer, layer conformally on the etching residues and the top surface of the patterned silicon layer*";

a method as recited in claim 7 and in particular comprising "*treating said patterned silicon layer with patterns and etching residues on sidewalls thereof using a gas comprising oxygen and a silicon etching agent to thereby form an etching buffer layer conformalty on the etching residues and the top surface of the patterned silicon layer*"; or

a method as recited in claim 14, and in particular comprising "*introducing a gas containing oxygen treatment, using a gas comprising oxygen and a silicon etching agent, to conformalty form an etching buffer layer on the etching residues and the top surface of the patterned silicon layer*".

Accordingly, in view of the above, Applicants submit that the Examiner has failed to show that a combination of Gardner, Ueda, the admitted prior art and Schloesser would have led one skilled in the art to a method as recited in Claims 1, 7 or 14. Applicants therefore respectfully submit that claims 1, 7 and 14 are patentable over Gardner in view of Schloesser, and that at least in view of their dependency on claims 1, 7 or 14, claims 4, 11 and 16 are patentable over Gardner in view of the admitted prior art and further in view of Schloesser.

* * *

In view of the above, Applicants submit that the application is now in condition for allowance and respectfully urge the Examiner to pass this case to issue.

The Commissioner is authorized to charge any additional fees that may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

March 2, 2007
(Date of Transmission)

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